What claimed is:

1. Driver stage for driving an output on one of n levels, which are each spaced from each other by a voltage difference of ΔV, comprising:

a plurality of field effect transistors for driving the output by leading a current to or away from the output,

with the relationship of the channel widths of at least two field effect transistors, which both act either for leading current to or away from, being set in dependence on the value of the voltage difference.

2. Driver stage in accordance with claim 1, further comprising:

a terminal circuit connected to the output and comprising a means for applying a terminal voltage and a terminal resistor connected in series between the means for applying a terminal voltage and an output.

3. Driver stage in accordance with claim 1, with the plurality of field effect transistors comprising:

a first and a second field effect transistor connected in parallel to each other between the output and a supply voltage, and

a third and fourth field effect transistor being connected in parallel to each other between the output and ground.

4. Driver stage in accordance with claim 1, further comprising:

a control means for turning the field effect transistors on and off, depending on a plurality of input bit signals in accordance with an allocation rule, which associates a selection of field effect transistors to be turned on and off with each bit combination of bit values of the input bit signals.

5. Driver stage in accordance with claim 1, wherein the at least two field effect transistors comprise two field effect transistors of the n-channel or p-channel type, which comprise a threshold voltage U_{th}, and, wherein the control means, in a bit combination, is implemented, so as to turn on a first one of the two field effect transistors and to turn the other off, in a different bit combination, to turn both field effect transistors on and, when turning on a respective one of the two field effect transistors, to apply a gate voltage U_G to a source/gate path of the respective one of the two field effect transistors, with the terminal voltage being roughly equal to half of the supply voltage, and the relationship being set in accordance with the following rule:

$$\frac{W_2}{W_1} = 3\,\frac{V_{DDQ} - \Delta V}{V_{DDQ} - 3\Delta V}\,\frac{4V_G - 4V_{th} - V_{DDQ} + \Delta V}{4V_G - 4V_{th} - V_{DDQ} + 3\Delta V} - 1$$

with W_1 being the transistor width of the first one of the two field effect transistors, W_2 being the transistor width of the other of the two field effect transistors, V_{DDQ} being the supply voltage, ΔV being the voltage difference, V_{th} being the threshold voltage and V_G being the predetermined source/gate voltage.

6. The driver stage in accordance with claim 1, wherein the at least two field effect transistors are operated in the linear range.

7. The driver stage in accordance with claim 1, wherein the relationship is greater than 2.

8. Method for manufacturing a driver stage for driving an output on one of n-levels, which are each spaced from each other by a voltage difference of ΔV, comprising the following steps:

forming a plurality of field effect transistors for driving the output by supplying or removing current to or from the output, with the relationship of the channel width of at least two field effect transistors, which both function to either lead current to or away, being set in dependence on the value of the voltage difference.

List of reference numbers

10	driver stage
12	push/pull-circuit part
12a	pMOS-transistor
12b	pMOS-transistor
12c	nMOS-transistor
12d	nMOS-transistor
14	transmission line terminal circuit part
14a	terminal resistor
14b	terminal resistor
14c	termination voltage terminal
14d	capacity
16	transcoder
18	transmission line
20	output
30	voltage axis